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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	PLW 13206
First Inventor or Application Identifier	Connolly
Title	CONTROL OF GAIN CURRENT SPREADING IN...
Express Mail Label No.	EF041512772US

09/710362 JC821 U.S. PTO 11/10/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231

1. [✓] *Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original, and a duplicate for fee processing)*
2. [✓] Applicant claims small entity status. See 37 CFR 1.27.
3. [✓] Specification *[Total Pages* 20 *]* *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [✓] Drawing(s) *(35 U.S.C. 113)* *[Total Sheets* 4 *]*
5. Oath or Declaration *[Total Pages* 3 *]*
   - a. [✓] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Form (CRF)
   - b. Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies); or
     - ii. [ ] paper
   - c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [ ] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [✓] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [✓] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: ____ / ____

Prior application information: Examiner ____ *Group / Art Unit* ____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

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FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	$382.00

Complete if Known	
Application Number	Herewith
Filing Date	Herewith
First Named Inventor	Connolly
Examiner Name	TBA
Group / Art Unit	TBA
Attorney Docket No.	PLW 13206

jc921 U.S. PTO 09/710060 11/10/00

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Deposit Account Name:

☐ Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR § 1.27

2. ☒ Payment Enclosed:

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	355.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	
				SUBTOTAL (1)	$355.00

2. EXTRA CLAIM FEES

	Extra Claims			Fee from below	Fee Paid
Total Claims	23	-20** =	3	X 9.00 =	27.00
Independent Claims	3	-3** =	0	X =	0.00
Multiple Dependent				=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) $27.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non - English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Statement	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

Reduced by Basic Filing Fee Paid SUBTOTAL (3)

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Jonathan M. Darcy	Registration No. (Attorney/Agent)	44,054	Telephone	(609) 987-6882
Signature	Jonathan M Darcy			Date	11/10/00

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"EXPRESS MAIL CERTIFICATE"

"Express Mail" mailing label number: EF041512772US

Date of Deposit: November 10, 2000

Title of Invention: CONTROL OF GAIN CURRENT SPREADING IN SEMICONDUCTOR LASER DIODES

Inventor: CONNOLLY, John C.; DIMARCO, Louis A.

Type of Documents:

1. Utility Patent Application Transmittal;
2. Fee Transmittal for FY 2000;
3. Application consisting of 14 pages of specification, 5 pages of claims, 1 page of Abstract, and 4 pages of drawings;
4. Declaration and Power of Attorney;
5. Our check in the amount of $382.00;
6. Acknowledgment Postcard; and,
7. "Express Mail" Certificate.

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Tammy T. Fattoross

CONTROL OF CURRENT SPREADING IN SEMICONDUCTOR LASER DIODES

Background of the Invention

This application claims the benefit of U.S. Provisional Application No. 60/164,864, filed November 12, 1999. The present invention relates to controlling the lateral extent of a region of a semiconductor laser diode that is exposed to a gain current, and specifically to controlling such lateral extent in a ridge waveguide semiconductor laser diode adapted to support selected lateral modes of the emitted laser light.

Summary of the Related Art

Typical semiconductor lasers such as laser diodes are formed by a body of semiconductor material having a thin, active region formed between cladding layers and contact regions of opposite polarity. A waveguide is formed in the structure by defining a stripe for light guiding and for current injection. Light is generated in the active region when the stripe region is subject to a current flow between the positive and negative contact regions. Cladding and confinement regions, among others, are placed between the contacts and the active region for guiding and confining the light along the thickness of the layers. The various regions typically are formed as substantially parallel thin layers grown epitaxially. When the current is greater than the threshold current for the active waveguide,

amplified light is generated. In general, the greater the current flowing into the active waveguide, the more light is generated.

The active regions can be shaped like a thin layer having a specified thickness, length and width. The oscillation of the electric and magnetic fields of the light waves are restricted to specific modes, depending on the dimensions of the active layer. The longitudinal mode of the light, along the direction of propagation, is determined by the longitudinal length of the active layer forming the laser cavity. Similarly, the thickness of the active layer restricts oscillation of the light waves in the transverse direction, perpendicular to the plane of the layers along which light propagates. By appropriately sizing the thickness of the layer, oscillations can be restricted to the fundamental mode or to other desired modes of the light.

However, in the lateral direction perpendicular to the length of the cavity and in the same plane as the layers, the modes are not limited by the size of the active layer, but rather by the width of the stripe and of the current flow region. More than one mode can thus co-exist simultaneously within the active layer.

One problem encountered in this type of semiconductor laser diode is that the light emitted may include more than one optical mode in the lateral direction, as described above. The multi mode light emitted from this type of diode is thus of limited use, because it is formed by a complex pattern of bright and dark areas. Many applications require laser light that has a far field pattern consisting of a single bright spot, made, for example, by light that includes only the fundamental

mode. For other uses, a different specific pattern can be required, such as one that is achieved by generating light having various selected modes.

A conventional method used to control the lateral modes of the light includes forming a positive conductor on top of the semiconductor layer, having a lateral dimension selected to only support the desired modes. An insulator can be placed between the active layer and the positive conductor layer outside of that lateral dimension, to prevent current flowing from the positive conductor outside of the selected region.

This method works for low power applications, but when the gain current flowing from the positive to the negative conductor and across the active layer exceeds a certain value, the current tends to spread in the lateral direction as it travels perpendicular to the layers. The degree of lateral current spreading can also increase with increased gain or drive current levels. This forms areas of high gain in the active layer that are larger than what is necessary to support the selected modes. When this occurs, extraneous modes can be supported by these enlarged gain areas of the active layer, and the light emitted is no longer of only the desired mode.

Accordingly, there is a need for a device and a method for controlling the lateral spread of current through an active layer of a semiconductor laser diode, so that the gain regions of the active layer can be limited in the lateral direction to only support desired lateral modes of the generated laser light, and in particular to support only the fundamental mode of the laser light.

Summary of the Invention

The present invention is directed to a semiconductor laser diode and a related method that is adapted to control the lateral modes of the laser light generated, so that only desired modes are supported. In particular, this result is achieved by controlling the lateral spread of the electric current that passes through the active layer, so that only a selected portion of the active layer has a high gain, resulting in amplification of only the light crossing that portion of the layer. The other portions of the active layer that flank the selected active region inhibit the flow of current, and therefore have a lower gain which results in less amplification, or no amplification of the light passing through those portions. The lateral dimensions of the high gain portion of the active layer can be selected to support only desired modes of the laser light, such as the fundamental mode or a combination of the fundamental and other modes.

The lateral control of the electric current is achieved by implanting high energy ions, such as protons, in the portions of the active layer that require a reduced conductivity, while shielding from the ion implant the portion of the active layer where high conductivity, therefore high gain is desired. This shielding can be obtained, for example, by placing a photoresist layer between the source of ions and the active layer. The photoresist layer can be shaped with openings that correspond to the size of the desired conductive portion of the active layer.

To achieve these and other advantages and in accordance with the purpose of the invention as embodied and broadly described, in one aspect the invention is

a ridge waveguide semiconductor laser diode adapted to support desired lateral modes of generated light, comprising a first conductor layer for application of a current, a second conductor layer facing the first conductor layer, an active layer disposed between the first and second conductor layers, a conduction region of the active layer adapted for conducting the current, and reduced conductivity regions of the active layer, flanking the conduction region, adapted to impede passage of the current.

Brief Description of the Drawings

The accompanying drawings are included to provide a further understanding of the invention, are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the objects, advantages and principles of the invention.

In the drawings:

Figure 1 is a schematic perspective view of one embodiment of a semiconductor laser diode incorporating the present invention;

Figure 2 is a schematic perspective view of the semiconductor laser diode shown in Figure 1, also including a barrier layer;

Figure 3 is a schematic front elevation view showing a detail of the embodiment of Figure 1; and

Figure 4 is a schematic view showing individual semiconductor laser elements disposed in an array.

Detailed Description of the Preferred Embodiments of the Invention

Semiconductor laser diodes are used in a variety of devices such as optical data storage and compact disc drives, for printing processes such as those used in laser printers, and also for displays. For certain applications, a plurality of laser diodes can be assembled in an array, so that the light from all of the arrayed laser diodes has the same mode and in some cases also the same phase.

For high brightness applications, a gain current up to 20 or 30 times the threshold current of the active layer in the laser diodes can be used to obtain a high brightness spot or beam from the semiconductor material.

Figure 1 shows one embodiment of a semiconductor laser diode according to the present invention. Semiconductor lasers consist of epitaxial layers grown on a single-crystal substrate 15. Typically, the substrate 15 is n-type. The exemplary semiconductor laser diode 1 has an active layer 10 that can include a quantum well structure. Active layer 10 can be formed, for example, of un-doped InGaAs or InGaAsP. A positive conductor 12 can be applied facing one surface of the active layer 10, and several p-type clad region layers and confinement layers can also be deposited in region 18, between the active layer 10 and the positive conductor 12, according to a conventional manner of construction of semiconductor laser devices. A negative conductor layer 14 can be formed on the

substrate 15, facing the opposite surface of active layer 10. A conventional arrangement of confinement layers and n-type clad layers can also be disposed in region 20, between the active layer 10 and the substrate 15.

Positive conductor layer 12 can be a strip as shown in Figure 1, or can extend the entire width of semiconductor laser diode 1. The strip shaped positive conductor layer 12 can preferably have dimensions corresponding to a region of active layer 10 that supports the desired optical modes. A dielectric insulator layer 16 can be used to prevent the flow of current from entering the top layers of region 18, outside of a selected lateral area. Insulator layer 16 thus defines an opening 17 in the insulator layer, that corresponds to the area where positive conductor 12 is in contact with region 18. In this manner, the current flowing from positive conductor 12 to negative conductor 14 is allowed to enter the portion of region 18 under opening 17, but is prevented from entering the remainder of region 18 by insulator layer 16. In a different embodiment, insulator 16 can be omitted from the device, particularly if positive conductor 12 is shaped as a strip of desired width, and does not extend the entire width of semiconductor laser diode 1.

The construction of semiconductor laser diode 1 can also include a ridged waveguide 22 extending parallel to a longitudinal axis of semiconductor laser device 1, and extending along the entire length L of the device. For example, ridge waveguide 22 can have a width of about 3 - 5 microns. Ridge waveguide 22 channels the light being emitted and amplified in active layer 10, so that the light

is directed for the most part along the longitudinal dimension of the semiconductor laser device 1.

In the lateral direction, along the active layer 10, the extent of the laser light is governed by the width of the waveguide, the lateral index step between the waveguide and the region external to it, and the amount of lateral current spread. In the case of a ridge waveguide, the lateral index step is the index difference between the region under the ridge 22, and the regions under the channels 23 on each side of the ridge 22.

If the index step is not present, the waveguide is "gain guided". In this case, the light is guided along the current path by virtue of the absorption difference, or gain vs. loss ratio, between the current flow region and its lateral regions. When the index step is present, the waveguide is "index guided", so that guiding of the light is achieved by the index step. Index guiding can be more advantageous than gain guiding, because it results in single-spatial mode operation and reduced astigmatism.

At low power settings, only a small portion of the active layer 10, approximately corresponding to the width of the non-insulated region of positive conductor layer 12, is crossed by the current. At high power settings, when the current flowing from positive conductor 12 to negative conductor 14 is relatively large, the combination of a stripe-like positive conductor 12 and an insulator 16 is insufficient to maintain the flow of current only within the general dimension of opening 17. Instead, the current tends to spread laterally outward to a region of

active layer 10 having greater width than the opening 17. The current thus no longer follows a straight line from positive conductor 12 to negative conductor 14, but instead flares laterally outwards, as schematically shown by the dashed line 31 in Figure 1. This broadens the effective width of the gain region generating light, and allows the waveguide to support additional lateral modes.

To prevent the occurrence of unwanted modes, active layer 10 is divided in a defined gain region 24 of high conductivity, through which the current flowing from positive conductor element 12 to negative conductor element 14 can easily pass, and flanking regions 26 of reduced conductivity, through which the current cannot easily pass. In this manner, the current flowing from positive conductor element 12 to negative element 14 is prevented from spreading laterally away from defined gain region 24, and follows a path shown by the solid line 32. The lateral dimension of the high gain portion of active layer 10 is thus limited to the size of defined gain region 24. By properly sizing the defined gain region 24, only the desired lateral modes of the laser light can be sustained, while other modes are not amplified and will decay.

For example, defined gain region 24 could be sized to only support the fundamental mode of the laser light in active layer 10, so that a sharp, single spot output laser beam can be generated by the device. Generation of laser light of the fundamental mode is useful for lasers used in telecommunications. For other applications, different modes can be useful. For example, a non-gaussian beam

formed by the fundamental and the second transverse mode can be useful in laser printing applications to improve printing sharpness.

The reduced conductivity regions 26 formed in the active layer 10 can be obtained, for example, by implanting ions such as protons in the material of active layer 10. The proton implant damages the structure of the active layer 10, and causes the affected region of active layer 10 to become non-conducting. The extent of the transformation incurred by active layer 10 is dependent on the strength and the duration of the proton implant. For example, successful results can be obtained by implanting protons having an energy of between approximately 130 KeV and 170 KeV. The implant can preferably have a duration of between about 1 and 5 minutes, and can be repeated more than once.

As shown in Figure 1, the laser light is amplified within a light amplification portion 30 of defined gain region 24. The actual shape of light amplification portion 30 depends on the desired mode being sustained. For example, in the case shown, the fundamental mode is supported, which results in a light amplification portion 30 shaped like a single elliptical spot through active layer 10, where the light amplification takes place.

The location within active layer 10 of reduced conductivity regions 26 must be selected carefully. The width of the defined gain region 24 of active layer 10 determines which lateral modes of the laser light will be supported, therefore reduced conductivity regions 26 must be placed sufficiently close to light

amplification portion 30 of active layer 10, so that additional modes will not be sustained by the active layer 10.

To satisfy these requirements, interface 40 between defined gain region 24 and reduced conductivity regions 26 must be selected to be just outside light amplification portion 30 of active layer 10. At the same time, interface 40 must not be so far from light amplification portion 30 that the defined gain region 24 can support modes other than the desired mode of the laser light.

The manufacturing process for semiconductor laser diode 1 will be described with reference to Figure 2. Positive and negative conductor layers 12 and 14, insulating layer 16, active layer 10 and the remaining layers forming semiconductor laser diode 1 are grown in a conventional manner. In a preferred embodiment of the device according to the present invention, reduced conductivity areas 26 are formed by implanting protons in the layers of the device. A source of protons 44 can be, for example, hydrogen.

A barrier layer such as photoresist layer 42 is used to shield from the protons areas of active layer 10 that are to remain conductive. For example, photoresist layer 42 can be placed above defined gain region 24, so that protons generated by source 44 are stopped by photoresist layer 42, and do not affect defined gain region 24. The remaining portions of the device, above and including the reduced conductivity regions 26, are implanted with protons, resulting in a loss of conductivity for those regions. In an embodiment according to the invention, only sections lying below the channels 23 on the sides of the ridge 22

are implanted. The depth of the implant can correspond approximately to the thickness of clad region 18 and can reach through active layer 10.

Figure 3 shows a detail of a region of the semiconductor laser depicted in Figure 1. This exemplary embodiment includes an implant region of constant depth 'd' obtained, for example, with an implant of given energy and duration. Because of the presence of channels 23 on the sides of ridge 22, the implant depth 'd' reaches active layer 10 in regions 26, below channels 23. Regions 26', located beyond channels 23, also receive an implant of depth 'd'. However, the layers of the laser diode above the active layer 10 have greater thickness at that point, and thus the implant in region 26' may not reach the active layer 10.

Figure 3 also shows lines 32 that indicate the path of current traveling through active layer 10 from positive conductor 12, and lines 33 indicating the path of spreading current blocked by reduced conductivity areas 26.

Protons from source 44 can travel across metallic layers and the various layers that form semiconductor laser diode 1, so that the proton implant can take place in a single step process, after all the layers of the wafer have been grown in a conventional manner. Photoresist layer 42 can be made, for example, of a long chain polymer such as SHIPLEY Photoresist Type AZ 4620, having a thickness of about 5 μm to 7 μm. However, other materials that absorb protons from source 44 can be used in photoresist layer 42.

Since the energy of the implant determines the amount of loss occurring in the implanted layer, the loss in selected regions of the active layer 10 can be

controlled with the location and energy of the implant. In this manner, the waveguide loss in the lateral direction can be selected by modifying the location of the implant. This loss introduced by the implant is another mechanism that can be used to control the laser light mode in the waveguide, in addition to controlling the current spread in reduced conductivity areas 26.

In a preferred embodiment, photoresist layer 42 can be placed above the outer surface of conductor layer 12, and can be removed after the implant has been performed. However, other configurations of photoresist layer 42 can be utilized, as long as photoresist layer 42 is placed between the source of protons 44 and the areas that are to remain conductive after the implant.

The semiconductor laser diode according to the invention is well suited for use in an array of laser diodes. For example, Figure 4 shows an exemplary array of individually-addressable laser elements 50. Each element 50 includes a ridge single-mode waveguide element 52, shown upside down in the figure. In an exemplary embodiment, a dielectric layer 54 and a p-side metallization layer 56 are formed with an appropriate shape and thickness to define the ridges 58. The

elements 50 are thermally and electrically separated by V-grooves 64, etched through the active region 60. In an exemplary embodiment, the element 50 are separated by approximately 50μm, resulting in an array that contains more than 200 laser elements, with a density of 50 elements per cm. All the laser elements in the exemplary embodiment produce a spot of laser light 62 in active layer 60 having the same mode characteristics.

It will be apparent to those skilled in the art that various modifications and variations can be made in the structure and the methodology of the present invention, without departing from the spirit or scope of the invention. Thus, the present invention is intended to encompass the modifications and variations that come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A ridge waveguide semiconductor laser diode adapted to support desired lateral modes of generated light, comprising:

a first conductor layer for application of a current;

a second conductor layer facing the first conductor layer;

an active layer disposed between the first and second conductor layers;

a defined gain region of the active layer adapted for conducting the current; and,

reduced conductivity regions of the active layer, flanking the defined gain region, adapted to impede passage of the current.

2. The semiconductor laser diode according to claim 1, further comprising at least one quantum wells layer formed in the active layer.

3. The semiconductor laser diode according to claim 1, wherein the defined gain region has a lateral extent adapted to support a desired lateral mode of the light.

4. The semiconductor laser diode according to claim 3, wherein the lateral extent supports a fundamental lateral mode.

5. The semiconductor laser diode according to claim 1, wherein the active

layer is formed of at least one of GaAs, InGaAs, AlGaAs, AlInGaAs and InGaAsP.

6. The semiconductor laser diode according to claim 1, wherein the first and second conductor layers are adapted to provide a current through the active layer that is larger than a threshold current of the active layer.

7. The semiconductor laser diode according to claim 1, wherein the defined gain region further comprises a light amplification portion sustaining the desired lateral modes, said light amplification portion having a smaller lateral extent than the defined gain region.

8. The semiconductor laser diode according to claim 1, wherein the reduced conductivity regions are implanted with high energy ions.

9. The semiconductor laser diode according to claim 8, wherein the reduced conductivity regions are implanted with protons of energy between about 130 KeV and 170 KeV.

10. The semiconductor laser diode according to claim 1, wherein the reduced conductivity regions provides a lateral index step.

11. The semiconductor laser diode according to claim 1, further comprising an insulator layer disposed adjacent the first conductor layer, for insulating a portion of the first conductor layer.

12. A method of forming a semiconductor laser diode providing controlled lateral diffusion of a gain current, comprising:

forming an active layer, a positive and a negative conductor layer;

disposing a barrier layer outside of the active layer, the barrier layer forming a mask defining an opening having a lateral dimension corresponding to a defined gain region; and

implanting high energy ions in the formed layers, the barrier layer being between a source of the high energy ions and the active layer during implanting.

13. The method according to claim 12, wherein disposing the barrier layer comprises disposing a photoresist layer.

14. The method according to claim 12, wherein the implanting step includes implanting protons having an energy of between about 130 KeV and 170 KeV.

15. The method according to claim 14, wherein the implanting step comprises implanting the protons for a time period of at least about 1 minute.

16. The method according to claim 15, wherein the implanting step comprises implanting the protons for a time period of about 5 minutes.

17. The method according to claim 12, further comprising selecting the lateral dimension of the opening to support a fundamental lateral mode of the light in the active layer.

18. The method according to claim 12, further comprising disposing said layer on an outer surface of the positive conductor layer.

19. A method of controlling lateral extent of a defined gain region of an active layer in a semiconductor laser diode, comprising:

forming a positive and a negative conductor layer facing respectively opposite surfaces of the active layer;

forming reduced conductivity regions of the active layer flanking the defined gain region of the active layer; and

passing a gain current through the defined gain region of the active layer between the positive and negative conductor layers, such that passage of the current outside of the defined gain region is impeded by the reduced conductivity regions.

20. The method according to claim 19, wherein the reduced conductivity

regions are formed by proton implanting.

21. The method according to claim 19, further comprising selecting dimensions of the defined gain region so that a desired mode of light is supported.

22. The method according to claim 21, wherein the desired mode is a fundamental mode of the light.

23. The method according to claim 19, further comprising forming an insulating layer between the active layer and one of the positive and negative conductor layers, said insulating layer having at least one opening corresponding to the defined gain region of the active layer.

Abstract of the Specification

A semiconductor laser diode and method are described, wherein the path of the current through the device between the positive and negative conductors is controlled. Lateral spread of the gain current in the active region is prevented by implanting protons in areas of the active layer flanking a desired gain region. The implanted regions become less conductive, and prevent lateral spread of the gain current. The position of the implanted regions can be selected so that the gain current only crosses a portion of the active layer that supports desired lateral modes of the laser light.

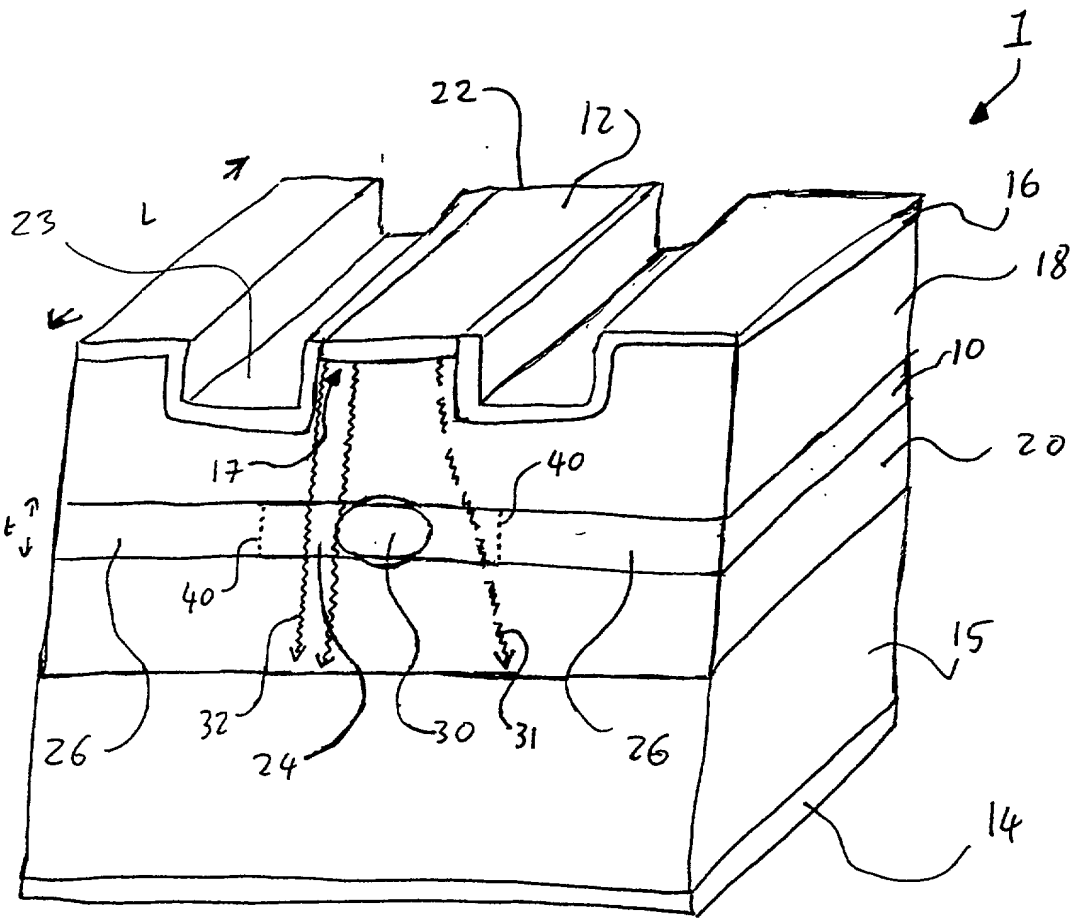

FIGURE 1

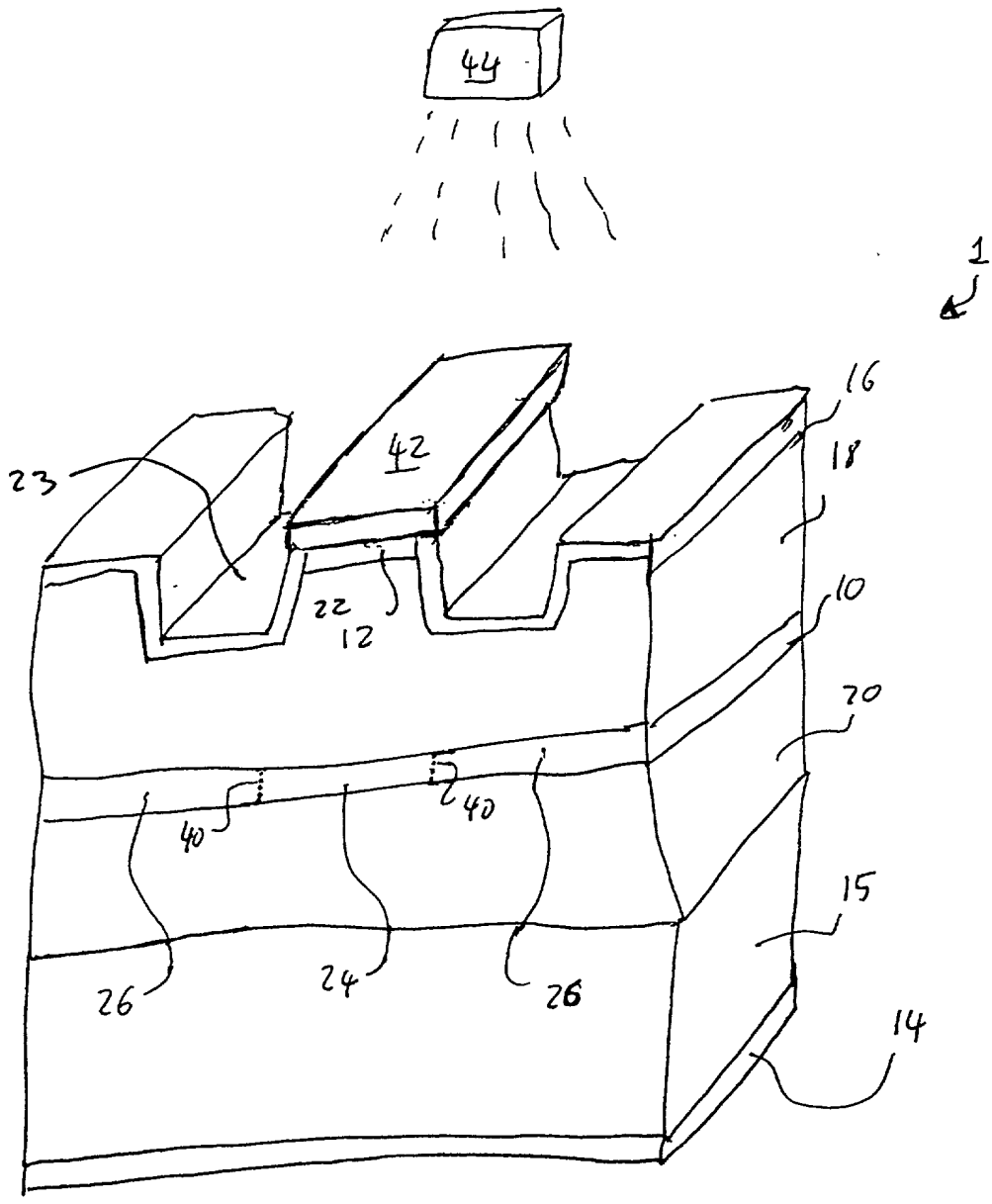

FIGURE 2

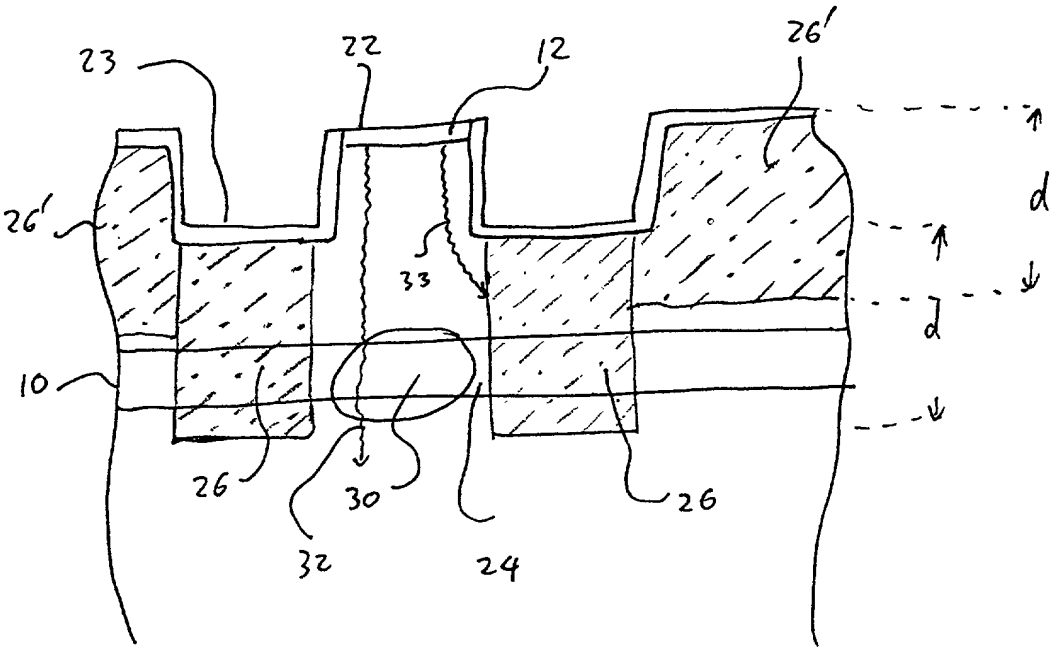

FIGURE 3

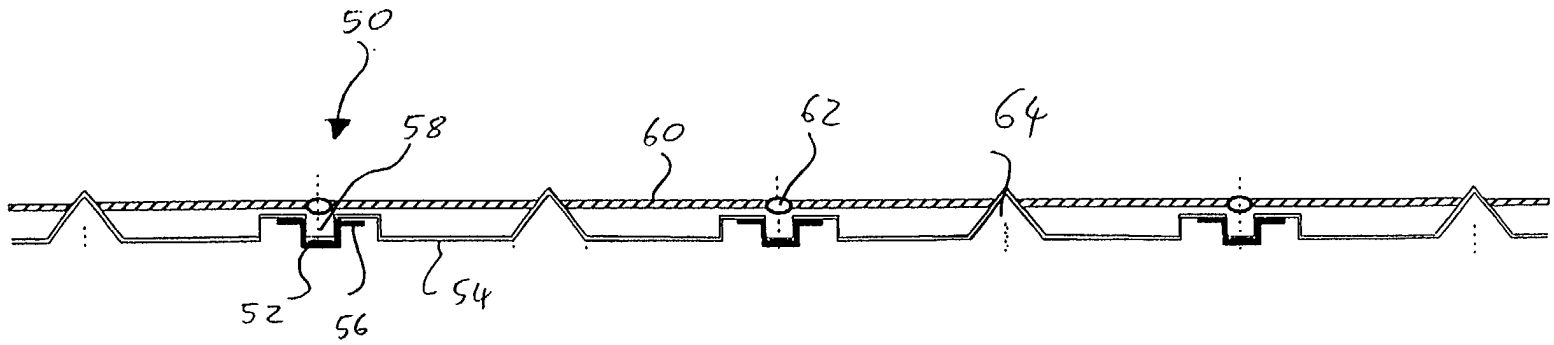

FIGURE 4

Docket No.
PLW 13206

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
CONTROL OF GAIN CURRENT SPREADING IN SEMICONDUCTOR LASER DIODES

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/164,864	November 12, 1999
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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